A New 7-Level Inverter for Active and Reactive Power Compensation Using PEV in Grid-Connected Applications

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Abstract – Typically, conventional multilevel inverters (MLI) have the disadvantage of being unable to step up the input voltage. Therefore, one type of three phase MLI with boost capacity is proposed. The proposed three-phase inverter is capable of generating seven levels (0, 1Vdc, 2Vdc, 3Vdc, -1Vdc, -2Vdc, -3Vdc), while only one DC source and five capacitors are required for the three phase configuration. To facilitate analysis, a phase position pulse-width-modulation (PD-PWM) strategy is applied to control switches. And suitable switching modes are also selected to balance the voltage of capacitors. In order to verify and validate the proper operation of the proposed circuit configuration and the ability using plug-in electric vehicle (PVE) battery into grid, the system is simulated in PLECS. The results of simulation are provided to validate the feasibility of the proposed inverter.

Keywords – Multilevel inverter, PVE, Vehicle-to-grid (V2G) application, Switched capacitor, PD-PWM.

I. INTRODUCTION

Multilevel inverter has been intensively studied in the literature for diverse range of applications, such as renewable energy conversion systems, high-voltage DC applications, and distributed generation systems. The application of V2G is one of the prospering new energy, which provide bi-directional power transmission between PVE batteries and the grid, and provide ancillary services to the grid. V2G can be applied in voltage regulation, frequency regulation and rotating reserve of the grid. In order to realized the application of V2G, the study of grid-connected inverters as well as control makes it possible [1]. Due to MLI's remarkable advantages such as near-sinusoidal output voltage waveform; low EMI, higher voltage power conversion [2]-[5]. There are three type of Conventional MLI topologies: the neutral-point-clamped (NPC) MLI, flying capacitor (FC) MLI and cascaded H-bridge (CHB) MLI [6]-[10]. These topologies have become remarkably mature in certain applications. For example, CHB MLI is extensively employed in photovoltaic (PV) systems, electric vehicles(EV), etc., which needs more H-bridge units to be cascaded for handling the higher power, resulting higher system costs [6]. On the other hand, FC MLI and NPC MLI are also well used in PV or EV system, driver applications. As the output level increasing, problems with voltage balance and failure rate of inverter are inevitable owing to the large number of components connected in the conventional inverter structures [7], [10].

Therefore, many researchers have made improvements based on conventional MLIs to obtain more competitive MLIs. Switched capacitor MLIs technology have the advantage of its flexible structure [10]. Hence, linking the switched capacitor structure with the conventional MLI structure became popular among researchers. in [12], a new type of active neutral clamp (ANPC) inverter can generate 7-levels is proposed. Additional voltage balancing circuits is required for this topology to balance the DC link capacitor's voltage, making the system more complicated. A hybrid 7-level ANPC topology is presented in [13], which used harmonic elimination to obtain an output voltage with lower harmonic distortion. However, the value of output voltage is smaller than the value of DC source, which means it has no boost capability. A 7-level inverter based on a T-type topology is introduced in [14] by using a floating capacitor unit to increase the number of output levels, but the output voltage is still half of the input voltage. As described above, the disadvantage the topology [12]-[14] is that additional circuit is required to regulate the floating capacitor's voltage.

To overcome these drawbacks mentioned above, resent topologies are proposed utilizing capacitor voltage self-balancing techniques to improve conventional MLI topologies. Two ANPC topologies with capacitor' voltage self-balancing capability and boosting capability have been presented in [15] and [16]. However, these topologies are still demanding a large number of switching elements and have a high DC link voltage.

With the aim of achieving a high gain, capacitor voltage self-balance and low-voltage stress, a new 7-level inverter based on a conventional T-type inverter is proposed. The proposed topology has a boost capacity of 1.5 times to the value of input voltage and more effectively utilizing the voltage of DC-link capacitors than conventional MLIs topology. Meanwhile, the proposed inverter fed by PVE's battery for compensating active and reactive power of the grid is verified using a power direct control strategy. The proposed topology is depicted in Fig.1, and simultaneous structural diagram of the grid-connected control block diagram is show in Fig.2.

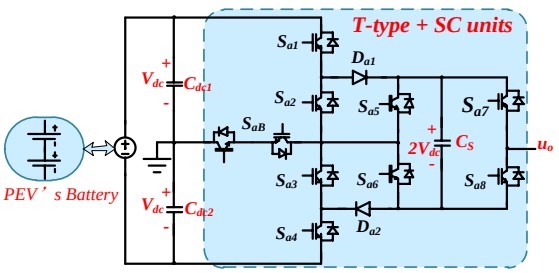


Fig.1: Proposed single phase of 7-level inverter

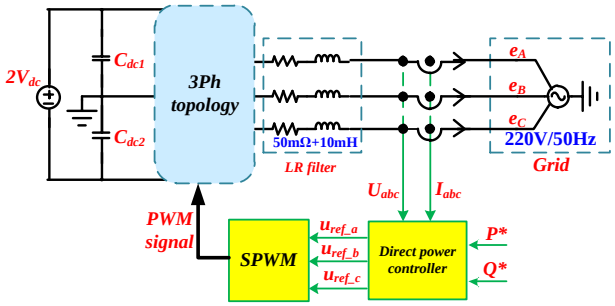


Fig.2: The schematic of direct power control strategy

II. Circuit Descriptions and Operating Principles

In order to facilitate the analysis, phase A is taken as an example for the following analysis. The phase A topology of the proposed seven-level boost inverter is depicted in Fig.1. the value of input voltage is $2V_{dc}$, u_o is equal to the output voltage, Cs is switched capacitor, C_{dc1} and C_{dc2} are the DC-Link capacitors. C_{dc1} has the same value as C_{dc2}, meaning that they have a uniform input voltage distribution. The switched capacitor is connected in parallel to the input voltage source through diodes D_{a1} and D_{a2}, which charge the voltage to the $+2V_{dc}$ at output voltage $\pm 1V_{dc}$. With the operation of switches S_{a1}-S_{a8} and S_{aB}, the proposed inverter is capable of generating seven-level voltage, and the maximum output voltage up to $+3V_{dc}$, thus achieving the boost capacity of 1.5 times. The states of switches and Cs for each output voltage are illustrated in Tab I.

As illustrated in Table I, this inverter is able to generate seven levels of 0, $\pm 1V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$. The state analysis of the positive half cycle (Mode 1-4) is shown in Fig.3.

Mode 4, the output level of the inverter is 0 as shown in Fig.3(a), the output terminal of the inverter is connected to the neutral ground through bidirectional switches S_{aB}, S_{a2}, D_{a1} and S_{a7}, and the other switching states as illustrated in Table I. The state of switched capacitor is idle.

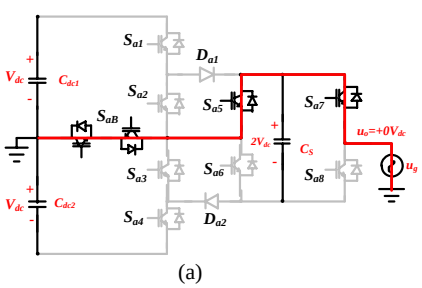
Mode 3, the output level of the inverter is $+1V_{dc}$ as shown in Fig.3(b), the output terminal of the inverter is connected to C_{dc1}'s positive terminal through the switches S_{a1}, D_{a1} and S_{a7}, and the other switching states as illustrated in Table I. The switched capacitor is connected in parallel with the input power supply. And its voltage is charged to $2V_{dc}$.

Mode 2, the inverter's output level is equal to $+2V_{dc}$ as illustrated in Fig.3(c), the inverter utilizes switched capacitor to provide energy output for the load through the bidirectional switch S_{aB}, S_{a6} and S_{a7}, which results in the switched capacitor's voltage drop. The other switching states is illustrated in Table I.

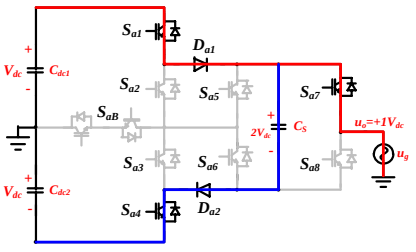
Mode 1, the inverter's output level is equal to $+3V_{dc}$ as illustrated in Fig.3(d), the switched capacitor is directly connected to C_{dc1} to provide energy output for the load through the bidirectional switch S_{aB}, S_{a1}, S_{a2}, S_{a6} and S_{a7}, which results the switched capacitor's voltage drop. The other switching states is illustrated in Table I.

Table 1: The working states for the phase A

Mode	Cs	Switching states			Output levels
		S_{aB}	S_{a1}~S_{a4}	S_{a5}~S_{a8}	
1	Discharge	0	1100	1010	$+3V_{dc}$
2	Discharge	1	0000	1010	$+2V_{dc}$
3	Charge	0	1001	0010	$+1V_{dc}$
4	Idle	1	0000	1010	$+0V_{dc}$
5	Idle	1	0000	0101	$-0V_{dc}$
6	Charge	0	1001	0001	$-1V_{dc}$
7	Discharge	1	0000	0101	$-2V_{dc}$
8	Discharge	0	0011	0101	$-3V_{dc}$



(a)



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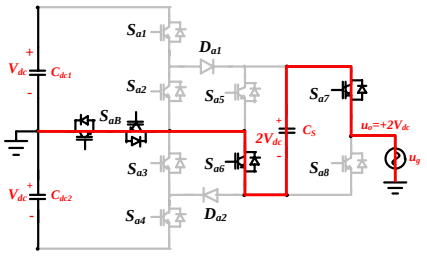
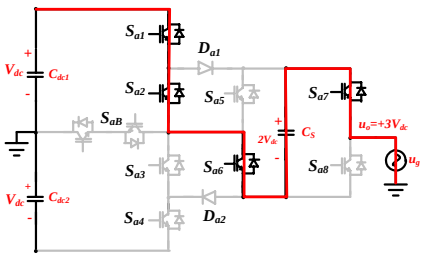


(c)



(d)

Fig.3: Operation modes of the proposed inverter: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4 .

III. Modulation and Capacitor Voltage Ripple

A. Modulation

In order to improve the quality of energy produced by MLIs, the fundamental frequency modulation or high frequency modulation can be used to make the inverter output sinusoidal voltage[10]. For the purpose of facilitating analysis, PD-PWM strategy is employed for the proposed multilevel circuits.

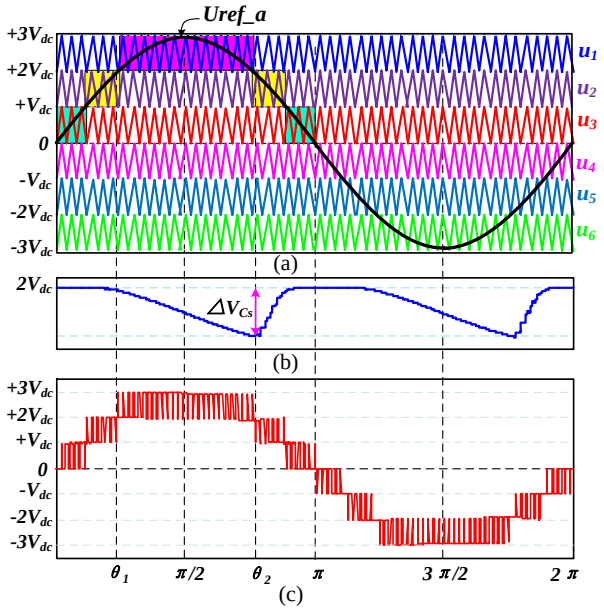


Fig. 4: The scheme of adopted PD-PWM.

Assume that the modulation waveform expression of phase A is :

$$u_{ref\_a} = 3V_{dc} \cdot m \cdot \sin(\omega t) \quad (1)$$

where m is the modulation index, $m \in (0,1)$.

As depicted in Fig.4(a), the PWM pulse of the switches is obtained by comparing the modulation signal(u_{ref_a}) with the carrier signals (u_1-u_6).

In Sector 1, reference waveform u_{ref_a} is compared with the carrier signal u_3 to generate an output level of 0 to $+1V_{dc}$.

In Sector 2, the modulation signal u_{ref_a} is compared with the carrier signal u_2 to generate an output voltage of $+1V_{dc}$ to $+2V_{dc}$.

In Sector 3, reference waveform u_{ref_a} is compared to the triangle signal u_1 to generate an output voltage from $+2V_{dc}$ to $+3V_{dc}$. Due to the symmetry of the modulation waveform, the principle of negative half cycle is the same as what was previously described. Eventually, the waveform of the output voltage waveform in phase A is shown in Fig.4(c).

B. Design Guideline of Capacitor

For the purpose of reducing the voltage ripple of *Cs* to enhance the power quality, it is essential to keep the voltage of *Cs* fluctuating within a certain range. During an output voltage of $\pm 3V_{dc}$, the capacitor *Cs* continuously provides energy to the load. When inverter output voltage is equal to $u_O = \pm 1V_{dc}$, *Cs* is in the state of charging and discharging alternately. When the output voltage is $0V_{dc}$,the *Cs* is connected in parallel with DC source. And *Cs* is in the state of idle. As is illustrated in Table 1.

As is shown in Fig.3(c), (d), the discharge current of *Cs* is the load current i_O, therefore, the amount of discharge of the capacitor *Cs* can be simply described as

$$\Delta Q = \frac{1}{C_s}\int_{t_1}^{t_2} i_O \, dt \quad (2)$$

where t_1 to t_2 is the duration of capacitor discharging time.

As shown in Fig. 4(b), for one cycle of the output voltage, the capacitor *Cs* has two continuous discharging periods i.e. $u_O = +2V_{dc}$. As a result, the amount of discharge ΔQ of C_S can be estimated by

$$\Delta Q = \frac{1}{2\pi f C_s}\int_{\theta_1}^{\theta_2} i_o d\omega t \quad (3)$$

where θ_1 and θ_2 are the conducting angle corresponding to $u_O = +2V_{dc}$, as depicted in Fig. 4(c); f is the frequency of the output voltage of proposed three-phase inverter .

Substituting $\theta_1 = \arcsin(2/3m)$ and $\theta_2 = \pi - \theta_1$ into (3), the expression can be derived as

$$\Delta Q = \frac{2V_{dc}}{2\pi f R C_s}\sqrt{9m^2 - 4} \quad (4)$$

It means that the amount of discharge is negatively correlated with frequency and load.

It can be further obtained from (4), the value of the capacitor *Cs* can be determined from the following equation within the allowable voltage ripple rating δ :

$$C_s = \frac{1}{\delta \pi f R}\sqrt{\left(\frac{3m}{2}\right)^2 - 1} \quad (5)$$

IV. Direct Power Control

To make the proposed inverter operate smoothly connected to the grid, a dual closed-loop controller is used to control the active and reactive power of proposed inverter in grid-connected application.

Assuming that the equivalent resistance of each phase on the output side of the grid-connected inverter and the grid-connected equivalent inductance are *R*, *L*,

respectively, the following relationship can be obtained from Fig.2 and the Kirchhoff voltage equation:

$$\begin{cases} u_A = Ri_A + L\dfrac{di_A}{dt} + e_A \\ u_B = Ri_B + L\dfrac{di_B}{dt} + e_B \\ u_C = Ri_C + L\dfrac{di_C}{dt} + e_C \end{cases} \tag{6}$$

where e_A , e_B, e_C are output voltage of grid.

The equation of the grid voltage in the d, q coordinate system can be obtained using the Park transform with rotation d, q coordinate system:

$$\begin{cases} u_d = Ri_d + L\dfrac{di_d}{dt} + e_d - L\omega i_q \\ u_q = Ri_q + L\dfrac{di_q}{dt} + e_q + L\omega i_d \end{cases} \tag{7}$$

In order to achieve complete decoupling of active and reactive power, and the PI controller is used to adjust the active and reactive currents. It is assumed that:

$$\begin{cases} \Delta u_d = Ri_d + L\dfrac{di_d}{dt} = PI({i_d}^*, i_d) \\ \Delta u_q = Ri_q + L\dfrac{di_q}{dt} = PI({i_q}^*, i_q) \end{cases} \tag{8}$$

Substitute equation (8) into equation (7), and the following equation is obtained:

$$\begin{cases} {u_d}^* = \Delta u_d - L\omega i_q + e_d \\ {u_q}^* = \Delta u_q + L\omega i_d + e_q \end{cases} \tag{9}$$

From the analysis above, the specific control strategy of the power external loop control of the grid-connected inverter can be obtained, as shown in Fig. 5.

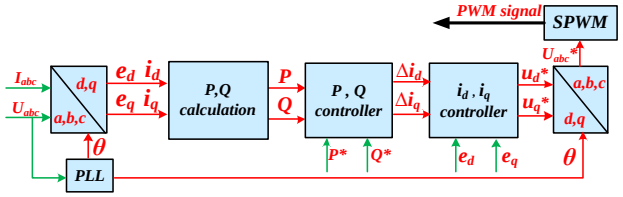


Fig. 5: The control strategy for grid-connected inverter

V. Simulation Results

To verify the feasibility of the proposed MLI and the stable operation of grid-connected control, a simulated model was created in PLECS referring Fig. 2. The system parameters are listed in Table2.

Condition 1: The voltage of 300V DC source is used in the simulation. the P* is equal to 1KW in 0 to 0.2s, 3KW in 0.2-0.5s, and 6KW in 0.5-1s. In order to make the proposed inverter operate in the unit power factor state with, i. e. the reactive power is equal to 0. The simulation results are presented in Figure 6(a), (b) and (c).

Table 2: Simulation of the system parameters

Parameter	Value
DC source $2V_{dc}$	***300V***
DC bus capacitors C_{dc}	***4000uF***
Capacitor Cs	***2000uF***
Filter R, L	***0.5ohm,10mH***
Grid phase voltage(RMS) e	***220V***
Grid frequency f	***50Hz***

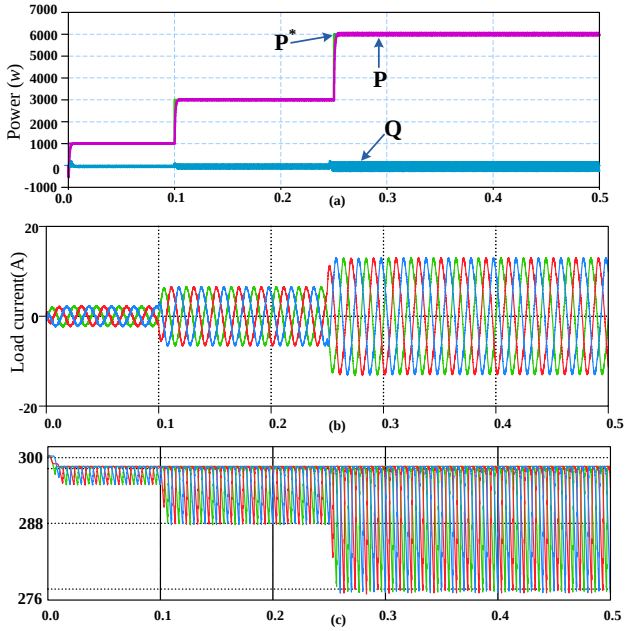


Fig. 6: The result of simulation: (a) *P*,*Q* under condition 1, (b) Load current waveform, (c) Voltage waveform of *Cs*

The results of the control of active P and active power Q are shown in Fig.6(a), and the waveform of three-phase grid current is shown in Fig.6(b). it can be clearly seen from Fig.6(a) that the active power output from the inverter is able to smoothly track the reference power when a given active power is suddenly change. Meanwhile, the load current can be quickly adjusted in response to changing output power of the inverter. The voltage ripple waveform of switched capacitor *Cs* is depicted in Fig.6(c). As proposed inverter's output power become large, the output current becomes larger which leads to larger ripple of the capacitor *Cs* at 0.1s and 0.25s, which verifies the section III.

Condition 2: The voltage of 300V DC source is used in the simulation. The active power is equal to 2KW from 0 to 0.2s, and then stepped up to 6KW at 0.2s. The reactive Q* is 0VAR at 0-0.3s, and then stepped up to 2000VAR at 0.3s. The other parameters are maintained identical. The simulation results are presented in Fig.7 (a), (b) and (c).

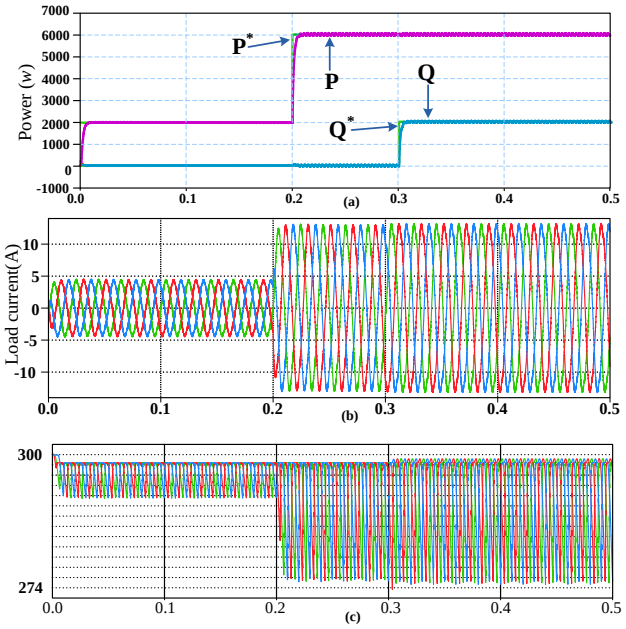


Fig. 7: The result of simulation: (a) *P*,*Q* under condition 2, (b) Load current waveform, (c) Voltage waveform of *Cs*

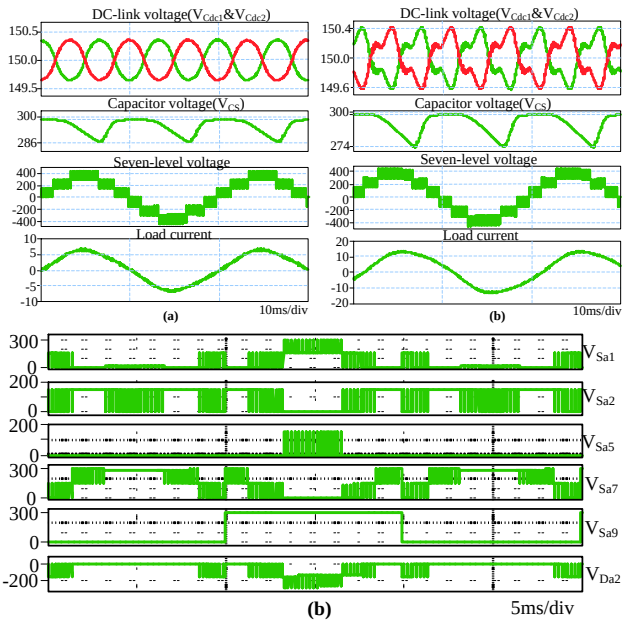


Fig. 8: Main waveforms of the proposed seven-level inverter : (a) Output voltage and current waveforms under condition 1, (b) Output voltage and current waveforms under condition 2, (c) Voltage waveform of witches and diode

The control results for active and active power are presented in Fig.7(a). The output current waveform of inverter is shown in Fig.7(b). The result that shown in Fig.7(a), (b) that the power provided by the proposed inverter can smoothly track the changes of a given power as the active power suddenly steps from 2KW to 6KW at 0.2s. Meanwhile, the inverter current can also be adjusted quickly. The ripple voltage of switched capacitor are shown in Fig.7(c), which indicates that the voltage ripple of the capacitor remains stable after a sudden change in the given reactive power, due to the inverter output current amplitude remaining constant.

Fig.8 shows the steady-state output voltage, the grid-connected current, and the voltage of the *Cs* and DC-link capacitor in the condition 1 (P=3000W). in the case that the power factor is equal to 1, the current and voltage are in phase. The voltage across the switched capacitor *Cs* and DC-link capacitor can be naturally balanced around its reference value, as shown is Fig.6(c) and Fig.8(a). Meanwhile, the inverter is also able to provide a stable output 7-level voltage. And the output voltage is 1.5 times the input DC voltage. When the system adds reactive power regulation, the voltages of the *Cs* and DC-link capacitor are also automatically balanced, as shown in Fig.7(c) and Fig.8(b). The devices voltage stress of the proposed topology, it can be seen that the voltage stress of topology's devices are less than or equal to input voltage.

V. Conclusion

In this paper, a type of three phase multilevel inverter with boost capacity is proposed for grid-connected application. The proposed inverter is introduced based on switched capacitor and T-type circuit structure. The switched capacitor is designed by theoretically analyzing so that the capacitor's voltage ripple stays within allowable limit. The power direct control strategy is also analyzed and designed to achieve the compensation of active and reactive power of the grid using PVE battery. The theoretical analysis is validated through simulation.

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